Docket No.: 51876P424

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

SOON-YONG KWEON

Art Group:

Application No.:

Examiner:

Filed:

For:

METHOD FOR FABRICATING FERROELECTRIC RANDOM ACCESS MEMORY DEVICE HAVING CAPACITOR WITH MERGED TOP-ELECTRODE AND

PLATE-LINE STRUCTURE

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure, enclosed is a copy of Information Disclosure Statement by Applicant (form PTO/SB/08), which is being submitted concurrently with the Utility Application. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

> -1-51876P424

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLI

Eric S. Hyman, Reg. No. 30,139

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Date: December 12, 2003

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51876P424

Complete if Known Substitute for form 1449A/PTO Application Number INFORMATION DISCLOSURE Filing Date Soon-Yong Kweon First Named Inventor STATEMENT BY APPLICANT Art Unit (use as many sheets as necessary) **Examiner Name** 2 1 Attorney Docket Number Sheet of 51876P424

U.S. PATENT DOCUMENTS									
inor		Document Number	Public	ation Date		Name of Patentee		Pages, Columns, Lines, When	re
Examiner Initials*	Cite No. ¹	Number - Kind Code² (if known)	or Iss	or Issue Date MM-DD-YYYY		Name of Patentee or Applicant of Cited Document		Relevant Passages or Relevant Figures Appear	
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Substitute for form 1449A/PTO INFORMATION DISCLOSURE				Complete if Known		
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INFO	RIVIA HON DI	SCLC	SURE	Filing Date		
STATEMENT BY APPLICANT				First Named Inventor	Soon-Yong Kweon	
				Art Unit		
(use as many sheets as necessary)				Examiner Name		
Sheet	2	of	2	Attorney Docket Number	51876P424	

NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No.¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²		
		Y NAGANO, et al., 0.18um SBT-Based Embedded FeRAM Operating at a Low Voltage of 1.1V, Symposium on VLSI Technology Digest of Technical Papers, 2003			
		Y.J. Song, et al., Highly Manufacturable and Reliable 32Mb FRAM Technology with Novel BC and Capacitor Cleaning Process, Symposium on VLSI Technology Digest of Technical Papers, 2003			

Examiner	Date	
Signature	Considere	d

Based on PTO/SB/08B (08-03) as modified by Blakely, Solokoff, Taylor & Zafman (wlr) 08/11/2003. Send To: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

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